Quantum-size effects in sub 10-nm fin width InGaAs FinFETs

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Abstracts

InGaAs FinFETs with sub-10 nm fin widths were fabricated for the first time using precision dry etching and digital etch. We find that the threshold voltage, V_T, becomes highly sensitive to the fin width, W_f, in the sub-10 nm W_f range. 2D Poisson-Schrodinger simulations suggest that this is due to quantization effects. We also show that in the quantum regime, a sidewall slope below 85^0 significantly reduce V_T variation at the same drawn dimensions.

Introduction

InGaAs has emerged as the most promising n-channel material for sub-10 nm CMOS [1]. In this dimensional range, only high aspect-ratio 3D transistors with a fin or nanowire configuration can deliver the necessary performance [2]. However, due to the low effective mass of InAs-rich III-V compounds, quantum effects are predicted to introduce great sensitivity of device characteristics to the fin width as it scales down to 7 nm and below [3]. In this work we fabricate InGaAs fin MOSFETs featuring fin widths in the sub-10 nm range and explore the role of quantum effects on V_T. We do indeed experimentally confirm the enhanced sensitivity of V_T to W_f, as compared with Si FinFETs with similar fin dimensions. The results have significant implications for future CMOS manufacturing.

Process technology

The FinFET process flow is illustrated in Fig. 1. This process closely follows that of [4]. In essence, this is an n-type doped-channel FinFET in which the gate modulates the electron concentration from the fin sidewalls only. The starting material consists of a 50 nm thick $In_{0.53}Ga_{0.47}As$ active layer Si-doped at 10^{18} cm^{-3} on an InAlAs buffer layer grown by MBE on SI-InP.

A novel reactive-ion etching process that utilizes a $BCl_3/SiCl_4/Ar$ chemistry has been used to create the fins [5]. HSQ defined by e-beam lithography is used as mask. Fins as narrow as 15 nm with an aspect ratio of 10 have been obtained [5]. 5 cycles of digital etch were used to reduce the fin width and smooth the sidewalls [6]. Our digital etch process consists of a self-limited plasma-oxidation/wet oxide etch sequence. In sample SW80 (SW90), the wet etch was done using H_2SO_4 (diluted-HCl). In both cases, digital etch reduces the fin width by ~2 nm/cycle while preserving its shape [5]. In our process, the sidewall slope at the top of the fin is related to the fin height and can be controlled by the fin etching time. Two different fin sidewall slopes were fabricated (Fig. 2). Sample SW90 has a fin height of 130 nm and vertical sidewalls at the top 50 nm. Sample SW80 has a fin height of 60 nm with a sidewall slope of ~80-85°. In this sample, W_f represents the dimension at the top of the fin. The bottom of the channel is enlarged by ~8 nm.

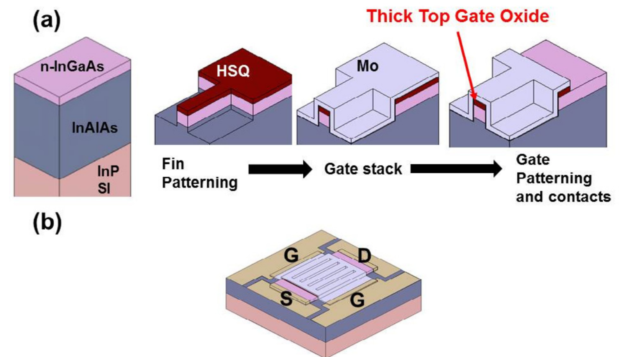

Fig. 1: (a) InGaAs FinFET process flow. (b) Finished device

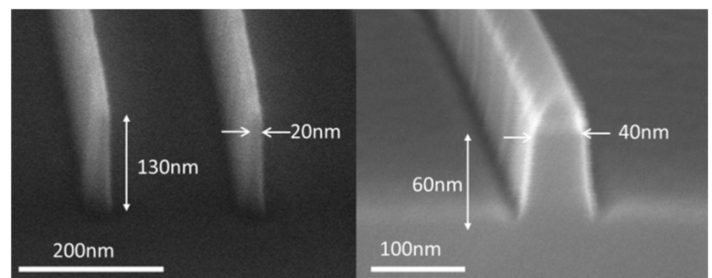

Fig. 2: Left: SW90 fins with vertical sidewalls. Right: SW80 fin with 80-85^0 sidewalls.

Immediately after digital etch, the sample is loaded into an ALD reactor for gate dielectric deposition. We used 5.5 nm of composite Al_2O_3/HfO_2 with EOT ~3 nm. Gating from the top facet of the fins is suppressed by leaving in place the HSQ mask (>10 nm thick) used to pattern the fins. The gate metal consists of sputtered Mo patterned by RIE. The gate covers the entire length of the fin and overlaps with the extrinsic regions. Evaporated Mo/Ti/Au is used for source and drain contacts

and pads. The final step is annealing in forming gas for 30 min at 400°C.

FIB cross-section of finished devices with sub-10 nm fins are shown in Fig. 3a-b. A typical device consists of 100 fins, 3 µm long (Fig. 4). W_f ranges between 5 and 35 nm.

Results

Output and subthreshold characteristics of a W_f=7 nm SW90 device are shown in Figs. 5-6. The current is normalized by the number of fins (100). Well-behaved long-channel behavior is obtained with negligible DIBL. This indicates excellent electrostatic charge control on the fin sidewalls.

Room temperature (RT) subthreshold characteristics at V_{DS}=50 mV for devices with different W_f are shown in Fig. 7a-b. A progressive positive V_T shift as W_f scales down is observed in both devices. V_T extracted at I_D=5 nA/fin is graphed in Fig. 7c-d. Sample SW90 exhibits an enhanced V_T dependence on W_f for values of W_f< 10 nm that is not observed in the SW80 sample.

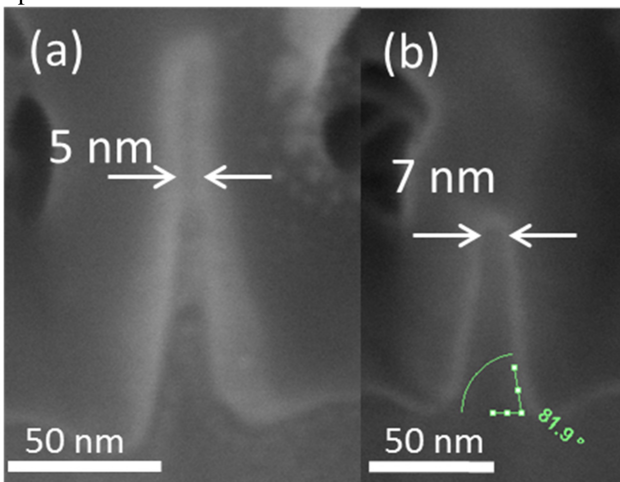

Fig. 3 FIB cross-sections of finished devices with **sub**-10 nm fins: (a) SW90 with vertical sidewalls, (b) SW80 with sloped sidewalls.

In order to understand the origin of this enhanced W_f dependence, we have carried out simultaneous I-V and C-V measurements at 90K at high frequency (500 KHz). This allows us to extract the mobility and sheet electron concentration while suppressing the impact of interface states. The temperature dependence of subthreshold characteristics of a typical device is shown in Fig. 8. V_T at 90K for both sets of devices is shown in Fig. 7c-d. Besides a nearly constant shift in V_T, low temperature brings a reduction in the V_T dependence for wide W_f. We attribute this to the reduced impact of interface states. However, the enhanced V_T dependence on W_f for very narrow SW90 devices remains at 90K.

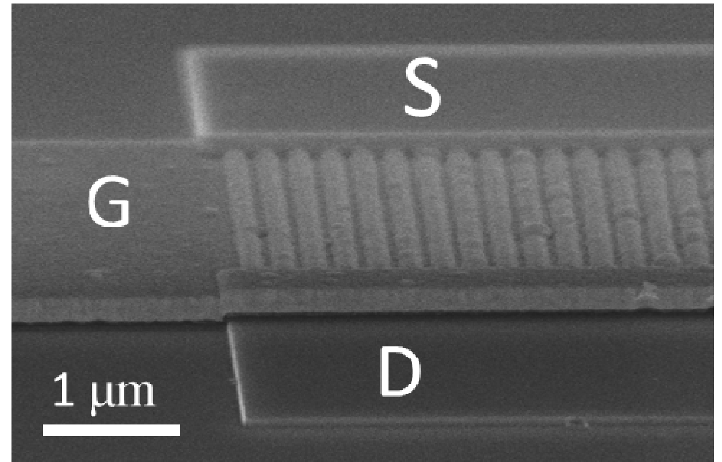

Fig. 4: SEM micrograph of a finished device.

The combination of C-V and I-V measurements (Figs. 9a and c) allows the extraction of the mobility, as shown in Fig. 9b at T=90K. For high enough carrier concentrations, a rather flat dependence of µ on n is observed as expected in a doped channel.

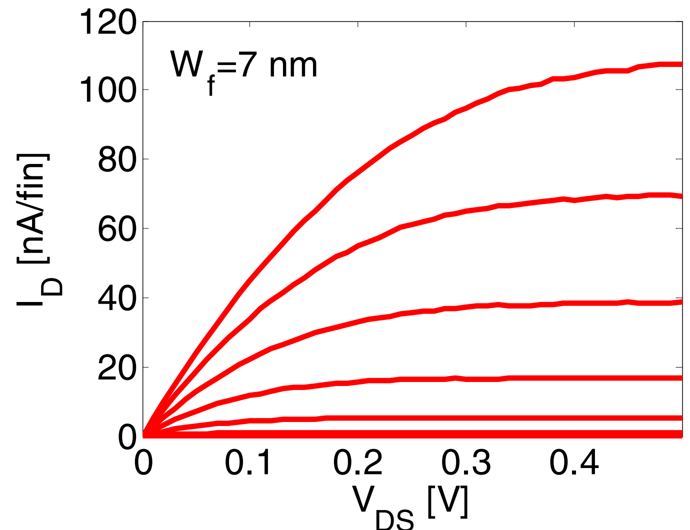

Fig. 5: Output characteristics of W_f=7 nm SW90 device. V_{GS} runs from 0 to 0.6 V in 0.1 V steps.

We estimate the electron concentration (n) in the subthreshold regime by using the mobility data obtained from CV-IV and the subthreshold current characteristics at 90 K. From this (Fig. 9d), we have extracted the threshold voltage, V_{Tn}, defined at a fixed carrier concentration of $5{\cdot}10^5$ cm^{-1} (Fig. 10). The SW80 data is characterized by a nearly constant slope while the SW90 samples with W_f<10 nm continue to exhibit an enhanced W_f dependence.

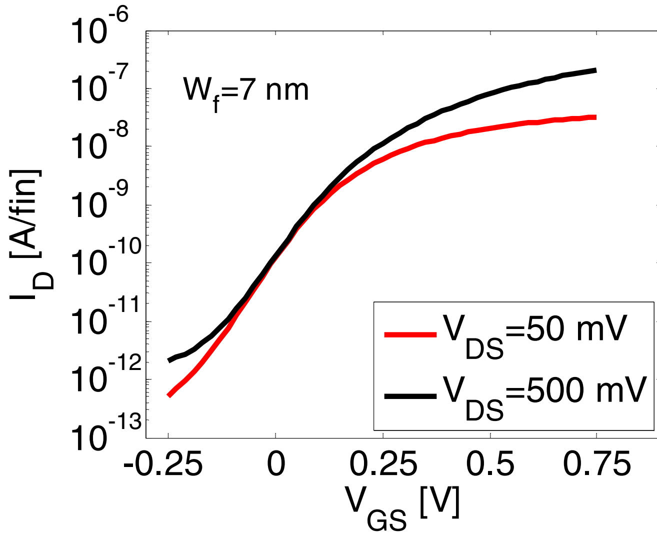

Fig. 6: Subthreshold characteristics of W_f=7 nm SW90 device.

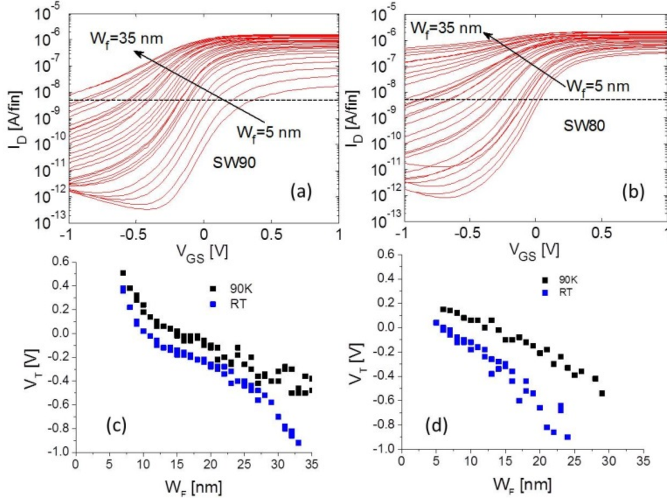

Fig 7: Room temperature subthreshold characteristics of devices with different W_f of SW90 (a) and SW80 (b). V_T as a function of W_f for SW90 (c) and SW80 (d) at room temperature and 90 K.

2D Poisson-Schrodinger simulations and discussion

In order to understand these experimental results, we have performed self-consistent 2D Poisson-Schrodinger simulations using Nextnano. Fig. 11 graphs V_{Tn} as extracted from these simulations at a fixed carrier concentration of $5x10^5 cm^{-1}$. On both types of devices, there is a clear steeper dependence of V_{Tn} on W_f in the sub-10 nm range. The dependence is more prominent in the structure with vertical sidewalls.

The origin of this can be understood by mapping the spatial distribution of electrons across the fins (Fig. 12). In the SW80 sample, the electron distribution peaks at the wide bottom of the fin while in the SW90 devices it has a narrower lamella shape that spans a large portion of the fin height. The enhanced steepness of V_{Tn} for W_f<10 nm in both samples arises from quantum effects. This can be seen by the classic V_T calculation shown in Fig. 11 that is successful in capturing the evolution of V_T in wider devices. The classic V_T is defined as the gate voltage that, within the depletion approximation, pinches off the fin. The P-S simulated V_{Tn} (shifted by 200 mV due to work function difference not accounted for in the simulations) is compared with the experimental results in Fig. 10 (full lines). The agreement gives us confidence in our interpretation.

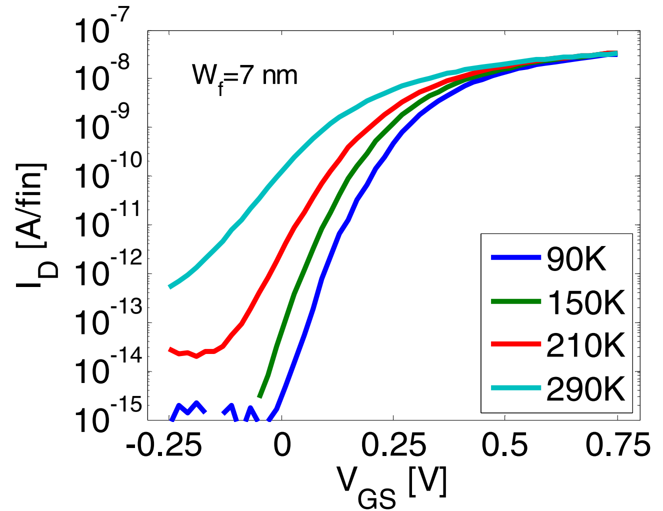

Fig 8: Transfer characteristics of W_f=7 nm SW90 device at different temperatures. V_{DS}=50 mV.

When all the data are plotted vs. the average W_f, the quantum size effects in both samples are equivalent (inset of Fig. 10).

The relevance of this work is highlighted by comparing the V_T dependence expected from P-S simulations in fins made out of different materials (Fig. 13). As a result of their low effective mass, quantum confinement effects in GaAs, InGaAs and InAs are much more significant than in Si. At W_f=5 nm, the sensitivity of V_T to W_f is 4 times higher for InGaAs than for Si. This implies that tight fin width control will be required in future InGaAs FinFETs and Trigate MOSFETs. In addition, the use of slanted sidewalls might help alleviate this issue though the consequences for charge control and short-channel effects need to be understood.

Conclusions

We demonstrate for the first time InGaAs FinFETs with sub-10 nm fin widths. In this dimensional range, we observe a strong dependence of V_T on fin width that is due to quantum confinement effects. This is far enhanced above Si-based devices due to the low effective mass of electrons in InGaAs. This has important implications for the design and manufacturing of future InGaAs MOSFETs.

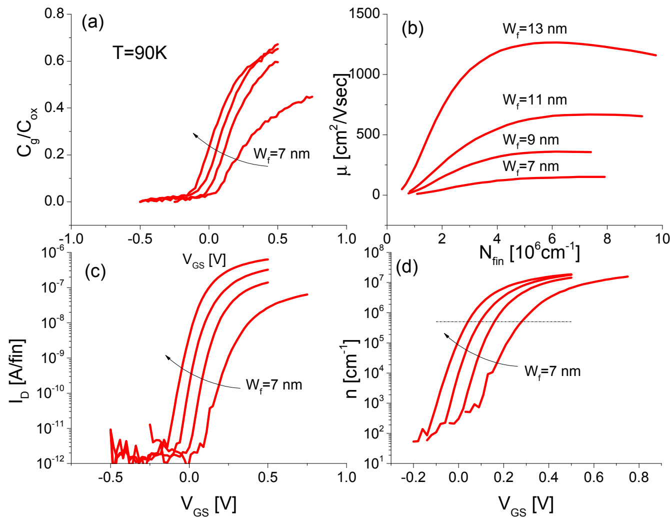
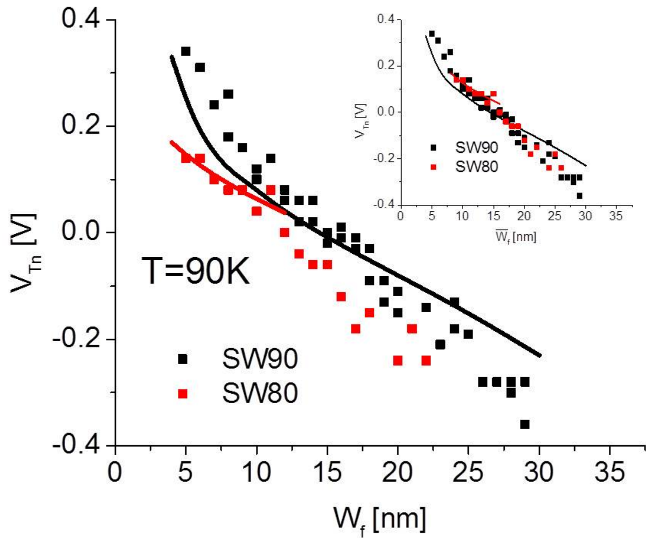
Fig 9: C-V (a) and I-V (c) characteristics of SW90 devices at V_{DS}=50 mV and T=90K. These are used to extract mobility (b). These measurements yield n-V_{GS} curves (d).

Fig 10: V_{Tn} (defined at n=5·10^5 cm^{-1}) vs. W_f. Lines: theory from Fig. 11 shifted by 0.2 V. Inset shows the same data plotted vs. average fin width.

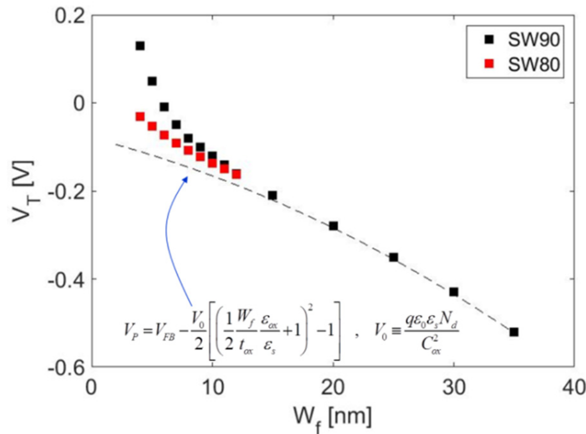

Fig 11: V_{Tn} as a function of W_f for SW90 and SW80 fins as extracted from 2D P-S simulations. Also included is V_T calculated using classic model.

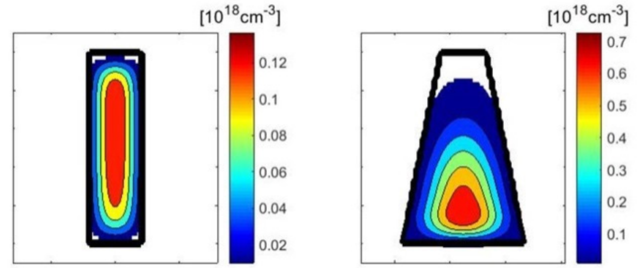

Fig 12: Electron density distribution at V_T for SW90 (left) and SW80 (right) fins. W_f=4 nm.

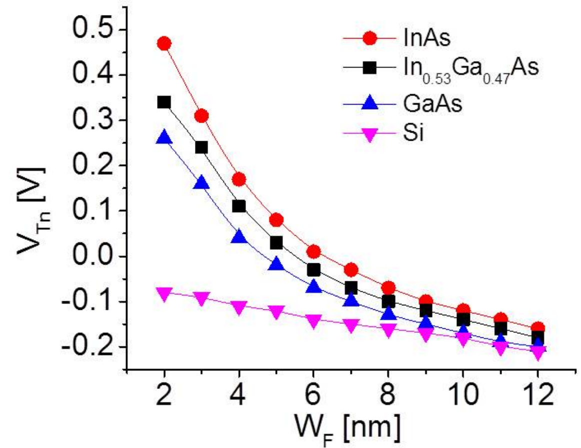

Fig 13: Simulated V_{Tn} vs. W_f for FinFETs with vertical sidewalls as obtained from 2D P-S simulations for different III-V semiconductors and comparison with Si.

Acknowledgment

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References

[1] J. A. del Alamo, "Nanometer-scale electronics with III-V compound semiconductors," in *Nature* vol. 479, pp. 317-323, 2011.

[2] K. J. Kuhn, "Considerations for ultimate CMOS scaling," in *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813-1828, Jul 2012.

[3] N. Agrawal Y. Kimura, R. Arghavani and S. Datta, "Impact of Transistor Architecture (Bulk Planar, Trigate on Bulk, Ultrathin-Body Planar SOI) and Material (Silicon or III–V Semiconductor) on Variation for Logic and SRAM Applications," in *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp 3298-3304, Oct 2013.

[4] A. Vardi, X. Zhao and J. A. del Alamo, "InGaAs Double-gate fin-sidewall MOSFET," in *IEEE Device Research Conf.* 2014.

[5] X. Zhao and J. A. del Alamo, "Nanometer-Scale Vertical-Sidewall Reactive Ion Etching of InGaAs for 3-D III-V MOSFETs," in *IEEE Electron Device Letters*, vol. 35, no. 5, pp. 521-523, May 2014.

[6] J. Lin, X. Zhao, D. A. Antoniadis and J. A. del Alamo, "A Novel Digital Etch Technique for Deeply Scaled III-V MOSFETs," in *IEEE Electron Device Letters*, vol. 35, no. 4, pp. 440-442, Apr 2014.